**Pentium Microprocessor**

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## 80486

The concepts of the **80386** microprocessor and the **80387** co-processor together evolved into the **80486** microprocessors. The only new advancement here was the introduction of the **8KB cache**.

The cache was used to store the most frequently used **data** and **instructions**. The cache is placed **closer** to the microprocessor, which reduces access time.

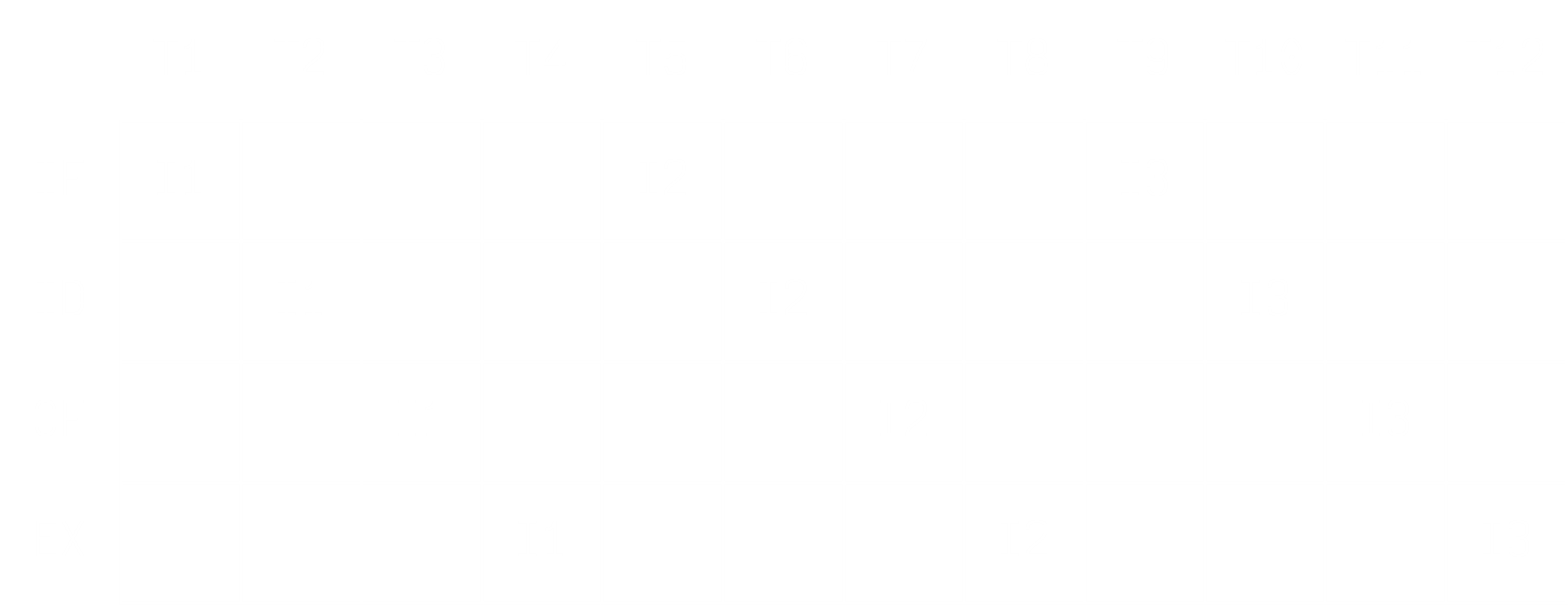
The **Pentium** microprocessor is an improvement to the architecture of the 80486 microprocessors.

## Improvements

* **Improved Cache Structure** - Pentium reorganized the cache structure to form **two level** (L2) caches, each of 8KB size. One of the caches was used to cache data, while the other was used to cache instructions.
* **Wider Bus Width** - The bus width was increased from 32 bits to **64 bits**.
* **Faster Numeric Processing** - The numeric processing was 5 times faster than that in the 80486 microprocessors. This was the result of the introduction of the **floating-point unit**.

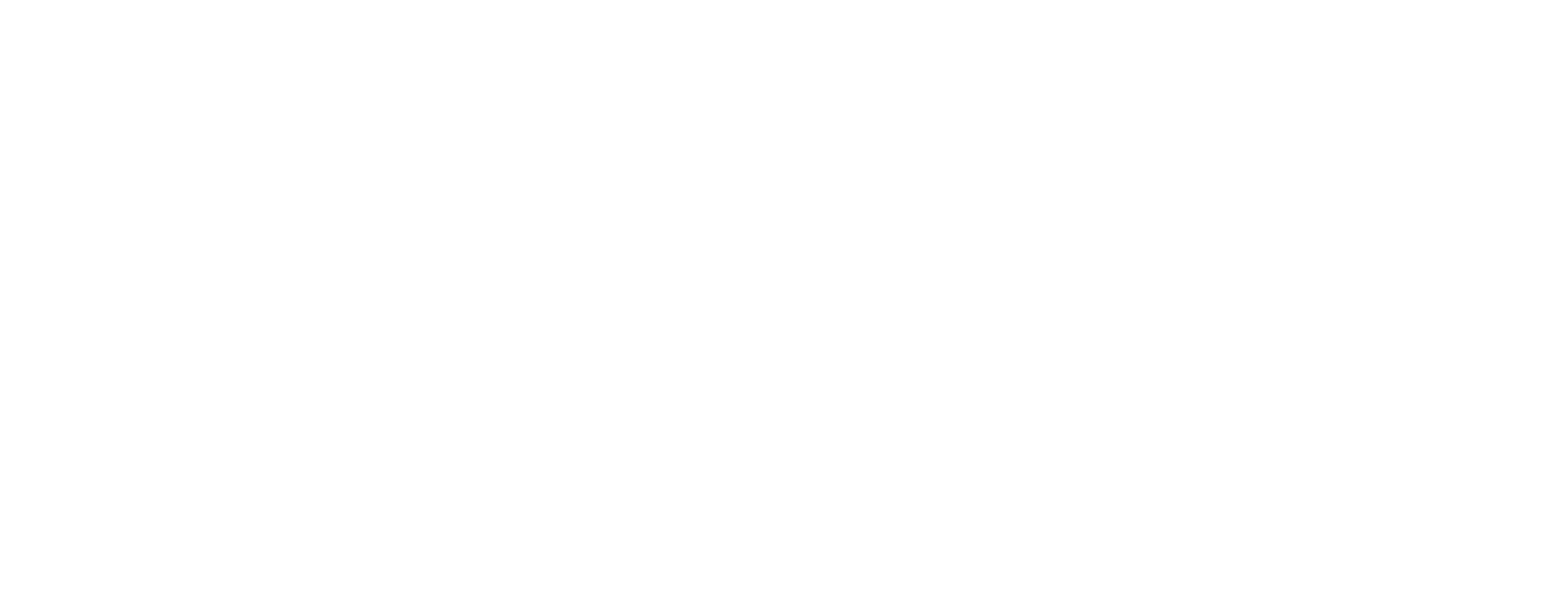
## Pipelining

Normally, microprocessors use **Sequential Processing**. There are four stages of executing an instruction, Instruction Fetch, Instruction Decode, Operand Fetch and Execution. In Sequential Processing, each instruction goes through these stages sequentially, something like the timing diagram below:



There is a lot of lost utilization under this process. To reduce that, **Pipelining** was introduced.

Under Pipelining, we can execute the operation of multiple stages for multiple instructions in overlapped time spans. This complicated definition just means that **different instructions** can now be in **different stages**, even if previous instructions have not completed execution.



Pentium has two **pipelines**:

* **U Pipeline** – This can execute **any Pentium instruction**, i.e. instructions that are specific to the Pentium processor.
* **V Pipeline** – This only executes **simple instructions**, i.e. general instructions that are not specific to the Pentium processor.

Each of the pipelines in Pentium has **5 stages**, unlike the four stages we saw for general pipelining above.

1. **Pre-Fetch** – Instructions are fetched from the Instruction Cache and placed in the prefetch buffer for decoding. This is done using the Prefetch unit.
2. **Instruction Decode** – Instructions are decoded into Pentium’s internal instruction format.
3. **Address Generation** – Address computations take place, which may take time if the real mode or virtual mode are being used.
4. **Execute, Cache and ALU Access** – The integer hardware executes the instruction.
5. **Write Back** – The results of the computation are written back to the register file. This stage is new in Pentium. It can take a while, since registers are huge, up to 80 bits.

## Super Scalar Machines

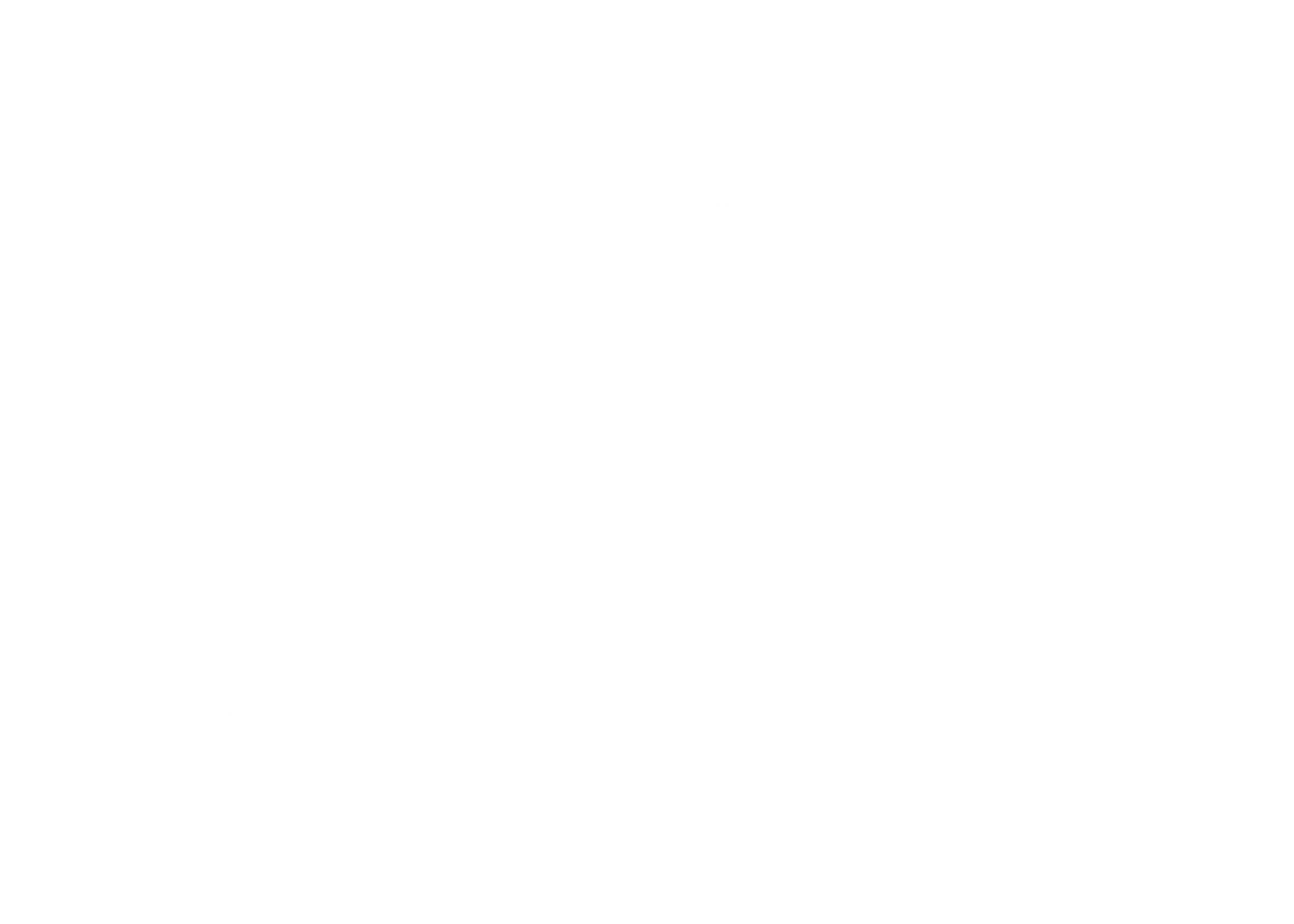
Any microprocessor that is capable of parallel instruction execution of multiple instructions is called a **super scalar machine**. Since Pentium has two execution lines, the U-line and the V-line, it is a super scalar microprocessor.

Technically, any microprocessor which exhibits one of the following properties can be considered a super scalar microprocessor:

* **Parallelism** – This is when instructions can have overlapping execution times, but not exactly the same start and finish time.
* **Simultaneity** – This is when instructions can be executed in parallel and also with exactly the same start and finish times.
* **Pipelining** – This is when both parallelism and simultaneity exist.

## Architecture

### Block Diagram



The Pentium microprocessor has all the units the 80386 microprocessors had, which includes:

* Instruction Unit
* Segmentation Unit
* Paging Unit
* Bus Unit
* Execution Unit

The **Execution Unit** holds the **U-Pipeline** and **V-Pipeline**.

### Floating-Point Unit

We have a new **Floating-Point Unit** in the Pentium microprocessor. It handles floating-point operations separately for the ALU.

It consists of **8 80-bit** general purpose **floating-point registers**, through . It also has an **8-stage pipeline**, the first five of which are the same as the U and V pipelines, and the three additional stages are:

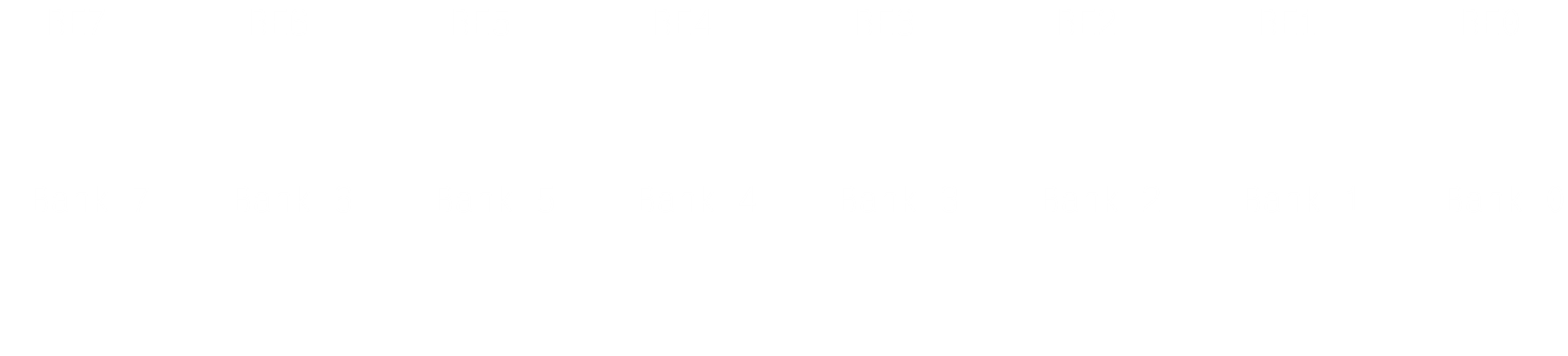
* First Execution Stage (XI Stage)
* Second Execution Stage (X2 Stage)
* Error Reporting Stage

The two additional execution stages are used to read data from the data cache and execute floating-point computations for the two portions of a floating-point number.

### Address Bus

The **Bus Unit** also has some differences. The **Data Bus** is now of **64 bits**, while the 32-bit **Address Bus** is now **bidirectional**. This is because I/O devices can access memory locations as well.

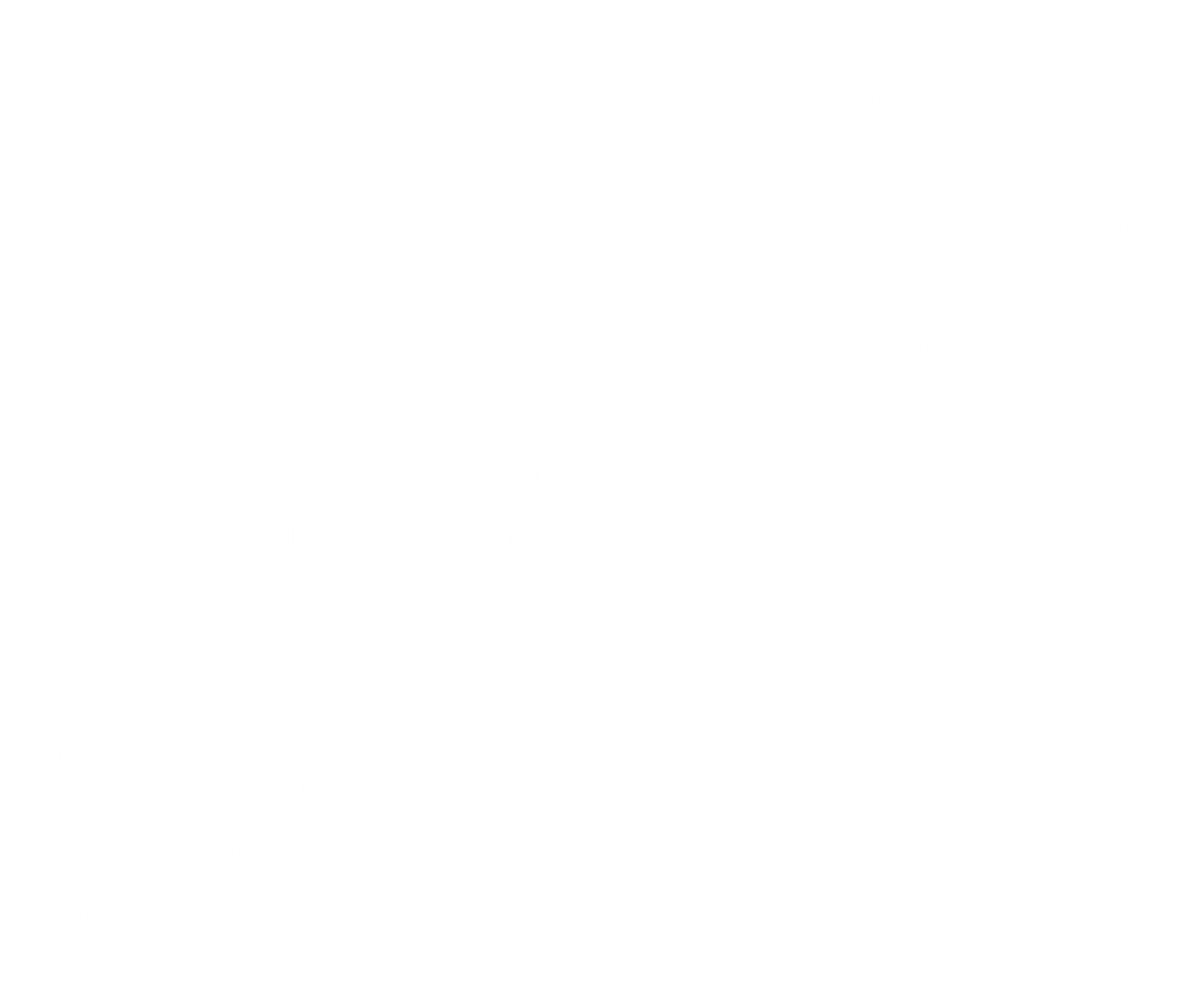
Only through are actually **address lines**. These work with the **byte-enable outputs**, to , to form the 32-bit address bus. Each byte-enable output enables access to a different **memory bank**. to are used to address the memory banks and are not directly available, but are internally decoded to produce the byte-enable outputs.



Each bank stores **1 byte** of data along with a **parity bit**, which helps with error detection and correction. This is a new capability in the Pentium processor.

With 32-bits, the maximum memory accessible is of **4GB**, with **65546 I/O ports**.

### Pin Diagram



There are 273 pins in Pentium, 64 for the Data Bus, to , 32 for the Address Bus, 75 for the Control Bus, 99 for VCC and Ground and 6 for No Connection.

## Pentium Pro

After the basic version of Pentium, **Pentium Pro** was created. This version had one notable difference, a **36-bit Address Bus**, allowing access to **64GB** memory. Even today, we do not have devices that use this much memory, so the allocation exists for future use.

There are **two versions** of Pentium Pro, one with a **256KB L2 cache** and another with a **512KB L2 cache**.

The microprocessor is packaged in a **387 pin** PGA (Pin Grid Array).

## Pentium II

After Pentium Pro came **Pentium II**. In this version:

* The **internal L2 cache** was moved out of the chip.
* It was not available as a **single chip**, but rather as a **plug-in circuit board**, called a **cartridge**, along with an **L2 cache chip**.

This also had various versions:

* **Celeron**, which did not have the L2 cache
* **Xeon**, which had up to 2MB of L2 cache

## Pentium III

**Pentium III** is based on the architecture of **Pentium Pro**, not Pentium II. Again, it is packaged as a **cartridge** instead of an IC chip.

A new feature is the inclusion of an **extra internal cache**, called a **Coppermine**, which was packaged in a **370-pin IC**. This is a fast cache with a **256KB advanced transfer mechanism** within the IC running at processor speed.

Notice how this is a 256KB cache instead of a 512KB one. This change was made because it was observed that a 512KB cache did not improve performance by much.

There are three versions of Pentium III:

* Standard
* **Celeron**, with a 66MHz bus speed
* **Xeon**, which allowed larger caches for server applications. This is still used for server processors.

## Pentium IV

Again, **Pentium IV** is based on the architecture of **Pentium Pro**. It is packaged in a **421-pin IC** and uses **physically smaller transistors**, which makes it both smaller and faster than the Pentium III. It was initially release with a 1.3GHz clock speed, but is now available with speeds of more than 3GHz.